Claims

We Claim:

1. A computer-implemented method for configuring a device to perform a measurement function, wherein the device includes a programmable hardware element, wherein the device also includes reconfigurable circuitry coupled to the programmable hardware element, the method comprising:

creating a block diagram in response to user input, wherein the block diagram specifies at least a portion of the measurement function;

generating a hardware architecture file based on at least a portion of the block diagram, wherein the hardware architecture file describes a hardware implementation of the at least a portion of the block diagram;

configuring the programmable hardware element in the device utilizing the hardware architecture file, wherein after said configuring the programmable hardware element implement a hardware implementation of the at least a portion of the block diagram;

configuring the reconfigurable circuitry in the device;

the device acquiring a signal from an external source after said configuring; and

the programmable hardware element and the reconfigurable circuitry in the device executing to perform the measurement function on the signal.

2. The method of claim 1,

wherein said configuring the reconfigurable circuitry comprises configuring the reconfigurable circuitry utilizing the hardware architecture file.

3. The method of claim 1, further comprising:

creating a reconfigurable circuitry configuration file which describes a configuration for the reconfigurable circuitry;

wherein said configuring the reconfigurable circuitry comprises configuring the reconfigurable circuitry utilizing the reconfigurable circuitry configuration file.

4. The method of claim 1,

wherein the block diagram includes a first portion that specifies a configuration for the programmable hardware element, and wherein the block diagram includes a second portion that specifies a configuration for the reconfigurable circuitry;

wherein said generating comprises generating the hardware architecture file based on the first portion of the block diagram; and

wherein said configuring the reconfigurable circuitry comprises configuring the reconfigurable circuitry based on the second portion of the block diagram.

5. The method of claim 1,

wherein the block diagram includes a first portion that specifies a configuration for the programmable hardware element, and wherein the block diagram includes a second portion that specifies a configuration for the reconfigurable circuitry;

wherein said generating comprises generating the hardware architecture file based on the first portion of the block diagram;

the method further comprising creating a reconfigurable circuitry configuration file based on the second portion of the block diagram, wherein the reconfigurable circuitry configuration file describes a configuration for the reconfigurable circuitry.

wherein said configuring the reconfigurable circuitry comprises configuring the reconfigurable circuitry utilizing the reconfigurable circuitry configuration file.

6. The method of claim 1, further comprising:

creating a second block diagram in response to user input, wherein the second block diagram specifies at least a portion of the measurement function;

creating a reconfigurable circuitry configuration file based on the second block diagram, wherein the reconfigurable circuitry configuration file describes a configuration for the reconfigurable circuitry;

wherein said configuring the reconfigurable circuitry comprises configuring the reconfigurable circuitry utilizing the reconfigurable circuitry configuration file.

7. The method of claim 1, wherein the reconfigurable circuitry comprises reconfigurable digital circuitry.

8. The method of claim 1, wherein the reconfigurable circuitry comprises reconfigurable analog circuitry.

9. The method of claim 1, wherein the reconfigurable circuitry comprises reconfigurable digital circuitry and reconfigurable analog circuitry.

10. The method of claim 1, wherein the device also includes a processor and memory coupled to the programmable hardware element;

the method further comprising:

storing an executable program in the memory of the device for execution by the processor on the device, wherein the executable program operates with the programmable hardware element and the reconfigurable circuitry to perform the measurement function.

11. The method of claim 1, wherein the device also includes a processor and memory coupled to the programmable hardware element;

wherein the hardware architecture file is based on a first portion of the block diagram;

the method further comprising:

generating an executable program based on a second portion of the block diagram;

storing the executable program in the memory of the device for execution by the processor on the device.

12. The method of claim 1, wherein the device is coupled to a computer system;

wherein said creating, said generating, and said configuring are performed in response to software executing on the computer system.

13. The method of claim 1, wherein the block diagram comprises a graphical program.

14. The method of claim 1, wherein the block diagram comprises a portion of a graphical program, wherein the graphical program also includes a display portion.

15. The method of claim 1, further comprising:

displaying one or more panels on a display during the programmable hardware element in the device executing to perform the measurement function on the signal, wherein at least one of the one or more panels displays the measured signal.

16. The method of claim 15,

wherein said displaying one or more panels comprises at least one of the one or more panels displaying output from the device during said executing.

17. The method of claim 15, further comprising:

receiving user input to at least one of the one or more panels during said executing;

providing the user input to the programmable hardware element; and

the programmable hardware element adjusting the measurement function on the signal in response to the user input.

18. The method of claim 15,

wherein the one or more panels comprise a user interface useable for viewing data generated by the device during the programmable hardware element in the device executing to perform the measurement function on the signal.

19. The method of claim 15,

wherein the one or more panels comprise a user interface useable for controlling the device and viewing output data from the device during the programmable hardware element in the device executing to perform the measurement function on the signal;

the method further comprising:

receiving user input to at least one of the one or more panels on the display to control the device during the programmable hardware element in the device executing to perform the measurement function on the signal.

20. The method of claim 15,

wherein the device is coupled to a computer system, wherein the computer system includes the display;

wherein said displaying comprises the computer system executing software to display the one or more panels on the display during the programmable hardware element in the device executing to perform the measurement function on the signal.

21. The method of claim 20,

wherein the block diagram comprises a portion of a graphical program, wherein the graphical program also includes a display portion;

wherein the display portion of the graphical program specifies the one or more panels;

the method further comprising:

compiling a portion of the graphical program corresponding to the one or more panels into executable code for execution by the computer system.

22. The method of claim 1,

wherein the device operates as an instrument;

wherein the external source is a unit under test.

23. The method of claim 1, further comprising:

at least one of the programmable hardware element and the reconfigurable circuitry generating a stimulus signal to the unit under test prior to the device acquiring the signal from unit under test.

24. A computer-implemented method for configuring a device to perform a measurement function, wherein the device includes a programmable hardware element, wherein the device also includes reconfigurable digital circuitry coupled to the programmable hardware element, the method comprising:

creating a block diagram in response to user input, wherein the block diagram specifies at least a portion of the measurement function;

generating a hardware architecture file based on at least a portion of the block diagram, wherein the hardware architecture file describes a hardware implementation of the at least a portion of the block diagram;

configuring the programmable hardware element in the device utilizing the hardware architecture file, wherein after said configuring the programmable hardware element implement a hardware implementation of the at least a portion of the block diagram;

configuring the reconfigurable digital circuitry in the device;

the device acquiring a signal from an external source after said configuring; and

the programmable hardware element and the reconfigurable digital circuitry in the device executing to perform the measurement function on the signal.

25. A computer-implemented method for configuring a device to perform a measurement function, wherein the device includes a programmable hardware element, wherein the device also includes reconfigurable analog circuitry coupled to the programmable hardware element, the method comprising:

creating a block diagram in response to user input, wherein the block diagram specifies at least a portion of the measurement function;

generating a hardware architecture file based on at least a portion of the block diagram, wherein the hardware architecture file describes a hardware implementation of the at least a portion of the block diagram;

configuring the programmable hardware element in the device utilizing the hardware architecture file, wherein after said configuring the programmable hardware element implement a hardware implementation of the at least a portion of the block diagram;

configuring the reconfigurable analog circuitry in the device;

the device acquiring a signal from an external source after said configuring; and

the programmable hardware element and the reconfigurable analog circuitry in the device executing to perform the measurement function on the signal.

26. A computer-implemented method for configuring a device to perform a measurement function, wherein the device includes a programmable hardware element, wherein the device also includes reconfigurable circuitry coupled to the programmable hardware element, the method comprising:

creating a first block diagram, wherein the first block diagram specifies a first portion of the measurement function;

creating a second block diagram, wherein the second block diagram specifies a second portion of the measurement function;

generating a hardware architecture file based on the first portion of the block diagram, wherein the hardware architecture file describes a hardware implementation of the first portion of the block diagram;

generating a reconfigurable circuitry configuration file based on the second portion of the block diagram, wherein the reconfigurable circuitry configuration file describes a configuration for the reconfigurable circuitry;

configuring the programmable hardware element in the device utilizing the hardware architecture file, wherein after said configuring the programmable hardware element implement a hardware implementation of the at least a portion of the block diagram;

configuring the reconfigurable circuitry in the device utilizing the reconfigurable circuitry configuration file;

the device acquiring a signal from an external source after said configuring; and

the programmable hardware element and the reconfigurable circuitry in the device executing to perform the measurement function on the signal.

27. A computer-implemented method for configuring a device to perform a measurement function, wherein the device includes a programmable hardware element, wherein the device also includes reconfigurable circuitry coupled to the programmable hardware element, the method comprising:

creating a block diagram, wherein the block diagram specifies the measurement function;

generating configuration information based on at least a portion of the block diagram, wherein the configuration information describes a hardware implementation of the at least a portion of the block diagram;

configuring the programmable hardware element and the reconfigurable circuitry in the device utilizing the configuration information, wherein after said configuring the programmable hardware element and the reconfigurable circuitry implement a hardware implementation of the at least a portion of the block diagram;

the device acquiring a signal from an external source after said configuring; and

the programmable hardware element and the reconfigurable circuitry in the device executing to perform the measurement function on the signal.

28. The method of claim 27,

wherein the configuration information includes a hardware architecture file;

wherein said configuring comprises configuring the programmable hardware element using the hardware architecture file.

29. The method of claim 27,

wherein the configuration information includes a reconfigurable circuitry configuration file;

wherein said configuring comprises configuring the reconfigurable circuitry using the reconfigurable circuitry configuration file.

30. The method of claim 27,

wherein the configuration information includes a hardware architecture file and a reconfigurable circuitry configuration file;

wherein said configuring comprises configuring the programmable hardware element using the hardware architecture file and configuring the reconfigurable circuitry using the reconfigurable circuitry configuration file.

31. A reconfigurable measurement system, comprising:

a computer system comprising a processor, memory and a display;

wherein the memory stores a block diagram, wherein the block diagram implements a measurement function;

wherein the memory also stores a software program which is executable to generate configuration information based on the block diagram, wherein the configuration information describes a hardware implementation of the block diagram; and

a device coupled to the computer system, wherein the device includes:

an input for acquiring a signal from an external source;

a programmable hardware element, wherein the programmable hardware element in the device is configurable utilizing the configuration information; and

reconfigurable circuitry coupled to the programmable hardware element, wherein the reconfigurable circuitry in the device is configurable utilizing the configuration information;

wherein after being configured the programmable hardware element and the reconfigurable circuitry implement a hardware implementation of the block diagram;

wherein the programmable hardware element and the reconfigurable circuitry are operable to perform the measurement function on an acquired signal.

32. The reconfigurable measurement system of claim 31,

wherein the configuration information includes a hardware architecture file;

wherein the programmable hardware element is operable to be configured using the hardware architecture file.

33. The reconfigurable measurement system of claim 31,

wherein the configuration information includes a reconfigurable circuitry configuration file;

wherein the reconfigurable circuitry is operable to be configured using the reconfigurable circuitry configuration file.

34. The reconfigurable measurement system of claim 31,

wherein the configuration information includes a hardware architecture file and a reconfigurable circuitry configuration file;

wherein the programmable hardware element is operable to be configured using the hardware architecture file, and wherein the reconfigurable circuitry is operable to be configured using the reconfigurable circuitry configuration file.

35. The reconfigurable measurement system of claim 31,

wherein the block diagram includes a first portion that specifies a configuration for the programmable hardware element, and wherein the block diagram includes a second portion that specifies a configuration for the reconfigurable circuitry;

wherein the configuration information includes a hardware architecture file and a reconfigurable circuitry configuration file;

wherein the software program is executable to generate the hardware architecture file based on the first portion of the block diagram; and

wherein the software program is executable to generate the reconfigurable circuitry configuration file based on the second portion of the block diagram.

36. The reconfigurable measurement system of claim 31, wherein the reconfigurable circuitry comprises reconfigurable digital circuitry.

37. The reconfigurable measurement system of claim 31, wherein the reconfigurable circuitry comprises reconfigurable analog circuitry.

38. The reconfigurable measurement system of claim 31, wherein the reconfigurable circuitry comprises reconfigurable digital circuitry and reconfigurable analog circuitry.

39. The reconfigurable measurement system of claim 31,

wherein the device also includes a processor and memory coupled to the programmable hardware element;

wherein the memory of the devices stores an executable program for execution by the processor on the device, wherein the executable program operates with the programmable hardware element and the reconfigurable circuitry to perform the measurement function.

40. The reconfigurable measurement system of claim 39,

wherein the software program is executable to generate the executable program based on the block diagram.

41. The reconfigurable measurement system of claim 31, wherein the block diagram comprises a graphical program.

42. The reconfigurable measurement system of claim 31, wherein the block diagram comprises a portion of a graphical program, wherein the graphical program also includes a display portion.

43. The reconfigurable measurement system of claim 31,

wherein the computer system is operable to display one or more panels on the display while the programmable hardware element and the reconfigurable circuitry in the device execute to perform the measurement function on the signal, wherein at least one of the one or more panels displays the measured signal.

44. The reconfigurable measurement system of claim 31,

wherein the software program is executable to select pre-existing configuration information based on the block diagram.

45. The reconfigurable measurement system of claim 31,

wherein the device operates as an instrument;

wherein the external source is a unit under test.

46. The reconfigurable measurement system of claim 45, wherein the device is operable to be coupled to a unit under test (UUT) in order to test the UUT;

wherein different types of UUTs may be coupled to the device;

wherein the device is reconfigurable to test the different types of UUTs.

47. The reconfigurable measurement system of Claim 45,

wherein different types of UUTs having various testing requirements may be coupled to the device;

wherein the reconfigurable measurement system is reconfigurable to test said different types of UUTs having said various testing requirements.

48. The reconfigurable measurement system of claim 31,

wherein the programmable hardware element comprises a Field Programmable Gate Array (FPGA).

49. The reconfigurable measurement system of claim 31,

wherein the reconfigurable circuitry comprises a Field Programmable Analog Array (FPAA).

50. The reconfigurable measurement system of claim 31,

wherein the reconfigurable circuitry comprises reconfigurable analog circuitry;

wherein the memory of the computer system stores a graphical analog design software program for designing an analog circuit diagram;

wherein the analog circuit diagram is used in creating a portion of the configuration information.

51. The reconfigurable measurement system of claim 31,

wherein the configuration information includes a reconfigurable circuitry configuration file;

wherein the reconfigurable circuitry is operable to be configured using the reconfigurable circuitry configuration file;

wherein the reconfigurable circuitry comprises reconfigurable analog circuitry;

wherein the memory of the computer system stores a graphical analog design software program for designing an analog circuit diagram;

wherein the analog circuit diagram is used in creating the reconfigurable circuitry configuration file.

52. The reconfigurable measurement system of claim 31,

wherein the reconfigurable circuitry comprises a Field Programmable Analog Array (FPAA);

wherein the memory of the computer system stores a graphical FPAA design software program for designing an analog circuit diagram;

wherein the analog circuit diagram is used in creating a portion of the configuration information.

53. The reconfigurable measurement system of claim 31,

wherein the memory of the computer system stores a graphical design environment for creating the block diagram.

54. The reconfigurable measurement system of claim 31,

wherein the block diagram comprises at least a portion of a graphical program;

wherein the memory of the computer system stores a graphical programming development environment for creating the block diagram.

55. The reconfigurable measurement system of claim 31,

wherein the block diagram comprises a data flow block diagram;

wherein the memory of the computer system stores a graphical data flow programming development environment for creating the data flow block diagram.

56. A computer-implemented method for configuring a device to perform a measurement function, wherein the device includes a programmable hardware element, wherein the device also includes reconfigurable circuitry coupled to the programmable hardware element, the method comprising:

creating a block diagram in response to user input, wherein the block diagram specifies at least a portion of the measurement function;

receiving user input specifying a first portion of the block diagram to be implemented in the programmable hardware element and a second portion of the block diagram to be implemented by the reconfigurable circuitry;

generating a hardware architecture file based on the first portion of the block diagram, wherein the hardware architecture file describes a hardware implementation of the first portion of the block diagram;

configuring the programmable hardware element in the device utilizing the hardware architecture file, wherein after said configuring the programmable hardware element implement a hardware implementation of the at least a portion of the block diagram;

configuring the reconfigurable circuitry in the device based on the second portion of the block diagram;

the device acquiring a signal from an external source after said configuring; and

the programmable hardware element and the reconfigurable circuitry in the device executing to perform the measurement function on the signal.

57. The method of claim 56, the method further comprising:

creating a reconfigurable circuitry configuration file based on the second portion of the block diagram, wherein the reconfigurable circuitry configuration file describes a configuration for the reconfigurable circuitry.

wherein said configuring the reconfigurable circuitry comprises configuring the reconfigurable circuitry utilizing the reconfigurable circuitry configuration file.

58. A computer-implemented method for configuring a device to perform a measurement function, wherein the device includes a programmable hardware element, wherein the device also includes reconfigurable circuitry coupled to the programmable hardware element, the method comprising:

creating a first block diagram in response to user input, wherein the first block diagram specifies a first portion of the measurement function;

creating a second block diagram in response to user input, wherein the second block diagram specifies a second portion of the measurement function;

receiving user input specifying the first block diagram to be implemented in the programmable hardware element and the second block diagram to be implemented by the reconfigurable circuitry;

generating a hardware architecture file based on the first block diagram, wherein the hardware architecture file describes a hardware implementation of the first block diagram;

configuring the programmable hardware element in the device utilizing the hardware architecture file, wherein after said configuring the programmable hardware element implement a hardware implementation of the at least a portion of the block diagram;

configuring the reconfigurable circuitry in the device based on the second block diagram;

the device acquiring a signal from an external source after said configuring; and

the programmable hardware element and the reconfigurable circuitry in the device executing to perform the measurement function on the signal.

59. The method of claim 58, wherein the second block diagram is a sub-diagram of the first block diagram.

60. A computer-implemented method for configuring a device to perform a measurement function, wherein the device includes a programmable hardware element, reconfigurable circuitry, and a processor and memory, the method comprising:

creating a block diagram in response to user input, wherein the block diagram specifies at least a portion of the measurement function;

receiving user input specifying a first portion of the block diagram to be implemented in the programmable hardware element, a second portion of the block diagram to be implemented by the reconfigurable circuitry, and a third portion of the block diagram to be implemented by the processor;

generating a hardware architecture file based on the first portion of the block diagram, wherein the hardware architecture file describes a hardware implementation of the first portion of the block diagram;

configuring the programmable hardware element in the device utilizing the hardware architecture file, wherein after said configuring the programmable hardware element implement a hardware implementation of the at least a portion of the block diagram;

configuring the reconfigurable circuitry in the device based on the second portion of the block diagram;

storing a software program based on the third portion of the block diagram in the memory for execution by the processor;

the device acquiring a signal from an external source after said configuring; and

the programmable hardware element, the reconfigurable circuitry, and the processor in the device executing to perform the measurement function on the signal.

61. A computer-implemented method for configuring a device to perform a measurement function, wherein the device includes a programmable hardware element, reconfigurable circuitry, and a processor and memory, the method comprising:

creating a first block diagram in response to user input, wherein the first block diagram specifies a first portion of the measurement function;

creating a second block diagram in response to user input, wherein the second block diagram specifies a second portion of the measurement function;

creating a third block diagram in response to user input, wherein the third block diagram specifies a third portion of the measurement function;

receiving user input specifying the first block diagram to be implemented in the programmable hardware element, the second block diagram to be implemented by the reconfigurable circuitry, and the third block diagram to be implemented by the processor and memory;

generating a hardware architecture file based on the first block diagram, wherein the hardware architecture file describes a hardware implementation of the first block diagram;

configuring the programmable hardware element in the device utilizing the hardware architecture file, wherein after said configuring the programmable hardware element implement a hardware implementation of the at least a portion of the block diagram;

configuring the reconfigurable circuitry in the device based on the second block diagram;

storing a software program based on the third block diagram in the memory for execution by the processor;

the device acquiring a signal from an external source after said configuring; and

the programmable hardware element, the reconfigurable circuitry, and the processor and memory in the device executing to perform the measurement function on the signal.

62. A computer-implemented method for configuring a device to perform a measurement function, wherein the device includes a programmable hardware element, reconfigurable circuitry, and a device processor and device memory, wherein the device is coupled to a computer system which includes a host processor and a host memory, the method comprising:

creating a block diagram in response to user input, wherein the block diagram specifies the measurement function;

receiving user input specifying a first portion of the block diagram to be implemented in the programmable hardware element, a second portion of the block diagram to be implemented by the reconfigurable circuitry, a third portion of the block diagram to be

implemented by the device processor, and a fourth portion to be implemented by the host processor;

generating a hardware architecture file based on the first portion of the block diagram, wherein the hardware architecture file describes a hardware implementation of the first portion of the block diagram;

configuring the programmable hardware element in the device utilizing the hardware architecture file, wherein after said configuring the programmable hardware element implement a hardware implementation of the at least a portion of the block diagram;

configuring the reconfigurable circuitry in the device based on the second portion of the block diagram;

storing a device software program based on the third portion of the block diagram in the device memory for execution by the device processor;

storing a host software program based on the fourth portion of the block diagram in the host memory for execution by the host processor;

the device acquiring a signal from an external source after said configuring; and

the programmable hardware element, the reconfigurable circuitry, the device processor, and the host processor executing to perform the measurement function on the signal.

63. A computer-implemented method for configuring a device to perform a measurement function, wherein the device includes a programmable hardware element, wherein the device also includes reconfigurable circuitry coupled to the programmable hardware element, the method comprising:

creating a block diagram in response to user input, wherein the block diagram specifies at least a portion of the measurement function;

executing a utility to automatically specify a first portion of the block diagram to be implemented in the programmable hardware element and a second portion of the block diagram to be implemented by the reconfigurable circuitry;

generating a hardware architecture file based on the first portion of the block diagram, wherein the hardware architecture file describes a hardware implementation of the first portion of the block diagram;

configuring the programmable hardware element in the device utilizing the hardware architecture file, wherein after said configuring the programmable hardware element implement a hardware implementation of the at least a portion of the block diagram;

configuring the reconfigurable circuitry in the device based on the second portion of the block diagram;

the device acquiring a signal from an external source after said configuring; and

the programmable hardware element and the reconfigurable circuitry in the device executing to perform the measurement function on the signal.

64. A computer-implemented method for configuring a device to perform an automation function, wherein the device includes a programmable hardware element, wherein the device also includes reconfigurable circuitry coupled to the programmable hardware element, the method comprising:

creating a block diagram in response to user input, wherein the block diagram specifies at least a portion of the automation function;

generating a hardware architecture file based on at least a portion of the block diagram, wherein the hardware architecture file describes a hardware implementation of the at least a portion of the block diagram;

configuring the programmable hardware element in the device utilizing the hardware architecture file, wherein after said configuring the programmable hardware element implement a hardware implementation of the at least a portion of the block diagram;

configuring the reconfigurable circuitry in the device;

the device acquiring a signal from an external source after said configuring;

the programmable hardware element and the reconfigurable circuitry in the device executing to perform the automation function on the signal; and

the device generating a control signal in response to said executing.

65. The method of claim 64,

wherein said configuring the reconfigurable circuitry comprises configuring the reconfigurable circuitry utilizing the hardware architecture file.

66. The method of claim 64, further comprising:

creating a reconfigurable circuitry configuration file which describes a configuration for the reconfigurable circuitry;

wherein said configuring the reconfigurable circuitry comprises configuring the reconfigurable circuitry utilizing the reconfigurable circuitry configuration file.

67. The method of claim 64,

wherein the block diagram includes a first portion that specifies a configuration for the programmable hardware element, and wherein the block diagram includes a second portion that specifies a configuration for the reconfigurable circuitry;

wherein said generating comprises generating the hardware architecture file based on the first portion of the block diagram; and

wherein said configuring the reconfigurable circuitry comprises configuring the reconfigurable circuitry based on the second portion of the block diagram.

68. The method of claim 64,

wherein the block diagram includes a first portion that specifies a configuration for the programmable hardware element, and wherein the block diagram includes a second portion that specifies a configuration for the reconfigurable circuitry;

wherein said generating comprises generating the hardware architecture file based on the first portion of the block diagram;

the method further comprising creating a reconfigurable circuitry configuration file based on the second portion of the block diagram, wherein the reconfigurable circuitry configuration file describes a configuration for the reconfigurable circuitry.

wherein said configuring the reconfigurable circuitry comprises configuring the reconfigurable circuitry utilizing the reconfigurable circuitry configuration file.

69. The method of claim 64, further comprising:

creating a second block diagram in response to user input, wherein the second block diagram specifies at least a portion of the automation function;

creating a reconfigurable circuitry configuration file based on the second block diagram, wherein the reconfigurable circuitry configuration file describes a configuration for the reconfigurable circuitry;

wherein said configuring the reconfigurable circuitry comprises configuring the reconfigurable circuitry utilizing the reconfigurable circuitry configuration file.

70. The method of claim 64, wherein the reconfigurable circuitry comprises reconfigurable digital circuitry.

71. The method of claim 64, wherein the reconfigurable circuitry comprises reconfigurable analog circuitry.

72. The method of claim 64, wherein the reconfigurable circuitry comprises reconfigurable digital circuitry and reconfigurable analog circuitry.

73. The method of claim 64, wherein the device also includes a processor and memory coupled to the programmable hardware element;

the method further comprising:

storing an executable program in the memory of the device for execution by the processor on the device, wherein the executable program operates with the programmable hardware element and the reconfigurable circuitry to perform the automation function.

74. The method of claim 64, wherein the device also includes a processor and memory coupled to the programmable hardware element;

wherein the hardware architecture file is based on a first portion of the block diagram;

the method further comprising:

generating an executable program based on a second portion of the block diagram;

storing the executable program in the memory of the device for execution by the processor on the device.

75. The method of claim 64, wherein the device is coupled to a computer system;

wherein said creating, said generating, and said configuring are performed in response to software executing on the computer system.

76. The method of claim 64, wherein the block diagram comprises a graphical program.

77. The method of claim 64, wherein the block diagram comprises a portion of a graphical program, wherein the graphical program also includes a display portion.

78. The method of claim 64, further comprising:

displaying one or more panels on a display during the programmable hardware element in the device executing to perform the automation function on the signal, wherein at least one of the one or more panels displays the measured signal.

79. The method of claim 78,

wherein said displaying one or more panels comprises at least one of the one or more panels displaying output from the device during said executing.

80. The method of claim 78, further comprising:

receiving user input to at least one of the one or more panels during said executing;

providing the user input to the programmable hardware element; and

the programmable hardware element adjusting the automation function on the signal in response to the user input.

81. The method of claim 78,

wherein the one or more panels comprise a user interface useable for viewing data generated by the device during the programmable hardware element in the device executing to perform the automation function on the signal.

82. The method of claim 78,

wherein the one or more panels comprise a user interface useable for controlling the device and viewing output data from the device during the programmable hardware element in the device executing to perform the automation function on the signal;

the method further comprising:

receiving user input to at least one of the one or more panels on the display to control the device during the programmable hardware element in the device executing to perform the automation function on the signal.

83. The method of claim 78,

wherein the device is coupled to a computer system, wherein the computer system includes the display;

wherein said displaying comprises the computer system executing software to display the one or more panels on the display during the programmable hardware element in the device executing to perform the automation function on the signal.

84. The method of claim 83,

wherein the block diagram comprises a portion of a graphical program, wherein the graphical program also includes a display portion;

wherein the display portion of the graphical program specifies the one or more panels;

the method further comprising:

compiling a portion of the graphical program corresponding to the one or more panels into executable code for execution by the computer system.

85. The method of claim 64,

wherein the device operates as a controller;

wherein the external source is a unit under test.

86. A reconfigurable automation system, comprising:

a computer system comprising a processor, memory and a display;

wherein the memory stores a block diagram, wherein the block diagram implements a automation function;

wherein the memory also stores a software program which is executable to generate configuration information based on the block diagram, wherein the configuration information describes a hardware implementation of the block diagram; and

a device coupled to the computer system, wherein the device includes:

an input for acquiring a signal from an external source;

an output for generating a control signal;

a programmable hardware element, wherein the programmable hardware element in the device is configurable utilizing the configuration information; and

reconfigurable circuitry coupled to the programmable hardware element, wherein the reconfigurable circuitry in the device is configurable utilizing the configuration information;

wherein after being configured the programmable hardware element and the reconfigurable circuitry implement a hardware implementation of the block diagram;

wherein the programmable hardware element and the reconfigurable circuitry are operable to perform the automation function on an acquired signal and generate a control signal in response thereto.

87. The reconfigurable automation system of claim 86,

wherein the configuration information includes a hardware architecture file;

wherein the programmable hardware element is operable to be configured using the hardware architecture file.

88. The reconfigurable automation system of claim 86,

wherein the configuration information includes a reconfigurable circuitry configuration file;

wherein the reconfigurable circuitry is operable to be configured using the reconfigurable circuitry configuration file.

89. The reconfigurable automation system of claim 86,

wherein the configuration information includes a hardware architecture file and a reconfigurable circuitry configuration file;

wherein the programmable hardware element is operable to be configured using the hardware architecture file, and wherein the reconfigurable circuitry is operable to be configured using the reconfigurable circuitry configuration file.

90. The reconfigurable automation system of claim 86,

wherein the block diagram includes a first portion that specifies a configuration for the programmable hardware element, and wherein the block diagram includes a second portion that specifies a configuration for the reconfigurable circuitry;

wherein the configuration information includes a hardware architecture file and a reconfigurable circuitry configuration file;

wherein the software program is executable to generate the hardware architecture file based on the first portion of the block diagram; and

wherein the software program is executable to generate the reconfigurable circuitry configuration file based on the second portion of the block diagram.

91. The reconfigurable automation system of claim 86, wherein the reconfigurable circuitry comprises reconfigurable digital circuitry.

92. The reconfigurable automation system of claim 86, wherein the reconfigurable circuitry comprises reconfigurable analog circuitry.

93. The reconfigurable automation system of claim 86, wherein the reconfigurable circuitry comprises reconfigurable digital circuitry and reconfigurable analog circuitry.

94. The reconfigurable automation system of claim 86,

wherein the device also includes a processor and memory coupled to the programmable hardware element;

wherein the memory of the devices stores an executable program for execution by the processor on the device, wherein the executable program operates with the programmable hardware element and the reconfigurable circuitry to perform the automation function.

95. The reconfigurable automation system of claim 94,

wherein the software program is executable to generate the executable program based on the block diagram.

96. The reconfigurable automation system of claim 86, wherein the block diagram comprises a graphical program.

97. The reconfigurable automation system of claim 86, wherein the block diagram comprises a portion of a graphical program, wherein the graphical program also includes a display portion.

98. The reconfigurable automation system of claim 86,

wherein the computer system is operable to display one or more panels on the display while the programmable hardware element and the reconfigurable circuitry in the device execute to perform the automation function on the signal, wherein at least one of the one or more panels displays the measured signal.

99. The reconfigurable automation system of claim 86,

wherein the software program is executable to select pre-existing configuration information based on the block diagram.

100. The reconfigurable automation system of claim 86,

wherein the device operates as a controller;

wherein the external source is a system being controlled.

101. The reconfigurable automation system of claim 86,

wherein the programmable hardware element comprises a Field Programmable Gate Array (FPGA).

102. The reconfigurable automation system of claim 86,

wherein the reconfigurable circuitry comprises a Field Programmable Analog Array (FPAA).

103. The reconfigurable automation system of claim 86,

wherein the reconfigurable circuitry comprises reconfigurable analog circuitry;

wherein the memory of the computer system stores a graphical analog design software program for designing an analog circuit diagram;

wherein the analog circuit diagram is used in creating a portion of the configuration information.

104. The reconfigurable automation system of claim 86,

wherein the configuration information includes a reconfigurable circuitry configuration file;

wherein the reconfigurable circuitry is operable to be configured using the reconfigurable circuitry configuration file;

wherein the reconfigurable circuitry comprises reconfigurable analog circuitry;

wherein the memory of the computer system stores a graphical analog design software program for designing an analog circuit diagram;

wherein the analog circuit diagram is used in creating the reconfigurable circuitry configuration file.

105. The reconfigurable automation system of claim 86,

wherein the reconfigurable circuitry comprises a Field Programmable Analog Array (FPAA);

wherein the memory of the computer system stores a graphical FPAA design software program for designing an analog circuit diagram;

wherein the analog circuit diagram is used in creating a portion of the configuration information.

106. The reconfigurable automation system of claim 86,

wherein the memory of the computer system stores a graphical design environment for creating the block diagram.

107. The reconfigurable automation system of claim 86,

wherein the block diagram comprises at least a portion of a graphical program;

wherein the memory of the computer system stores a graphical programming development environment for creating the block diagram.

108. The reconfigurable automation system of claim 86,

wherein the block diagram comprises a data flow block diagram;

wherein the memory of the computer system stores a graphical data flow programming development environment for creating the data flow block diagram.